AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A data processing system comprising:

an erasable and programmable non-volatile memory; and

a central processing unit[[;]]~

~~wherein the central processing unit executes a predetermined process to thereby carry out a process for increasing the number of assurances for rewriting in a specified partial storage area of the non-volatile memory as compared with the number of assurances for rewriting in other storage areas of the non-volatile memory~~

wherein in a first write operation for writing first data into a first area of said memory, the central processing unit writes the first data to a first portion of said first area,

wherein in a second write operation for writing second data into a second area of said memory, the central processing unit writes the second data to a portion of said second area, and

wherein the central processing unit writes supplemental information relating to the first data into a second portion of said first area in said first write

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operation, but does not write such supplemental information relating to the second data in said second write operation.

2.   (Currently Amended) A data processing system comprising:

an erasable and programmable non-volatile memory; and

a central processing unit;

wherein the central processing unit executes a predetermined process to thereby generate error correcting information and add the same to data to be written [[in]] only for a specified partial storage area of the non-volatile memory and allow an error decision and an error correction based on the error correcting information to be effected on the data read from the specified partial storage area.

3.   (Currently Amended) The data processing system according to claim 2, which is a single chip type microcomputer wherein the non-volatile said memory and the central processing unit are formed on a single semiconductor chip.

4.   (Currently Amended) The data processing system according to claim 2, which is configured in a multi-chip form wherein the non-volatilesaid memory and the central processing unit are respectively formed on discrete semiconductor chips.

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5.   (Original) The data processing system according to claim 2, wherein the predetermined process comprises an error-correcting information generating program for generating error correcting information for the data written into the specified partial storage area of the non-volatile memory, and an error-correcting program for effecting an error decision and an error correction on data with error correcting information read from the specified partial storage area.

6.   (Original) The data processing system according to claim 5, which has a storage area for a matrix table wherein when the data is configured as n bits and error correcting information for the n-bit data is defined as m bits, mutually-different binary numbers of m bits are arranged in an m+n array, and wherein the matrix table is referred to the error-correcting information generating program and the error-correcting program.

7.   (Original) The data processing system according to claim 5, further including a mask ROM accessible by the central processing unit, and wherein the mask ROM has the error-correcting information generating program and the error-correcting program.

8.   (Original) The data processing system according to claim 5, wherein the other storage areas of the non-volatile memory have areas for storing the error-correcting

information generating program and the error-correcting program.

9. (Original) The data processing system according to claim 8, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed, and the areas for storing the error-correcting information generating program and the error-correcting program are assigned to the erase prohibition area.

10. (Original) The data processing system according to claim 9, wherein the error-correcting information generating program serves so as to generate error correcting information and thereafter store the generated error correcting information and data corresponding thereto in the specified partial storage area in accordance with a prescribed format as data with the error correcting information, and the error-correcting program serves so as to recognize the data with the error correcting information in accordance with the prescribed format.

11. (Currently Amended) The data processing system according to claim 8, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite

allowable area in which erasing and writing are allowed, and

        wherein the areas for storing the error-correcting information generating program and the error-correcting program are assigned to the rewrite allowable area.

12.   (Original) The data processing system according to claim 5, further including a RAM to which the error-correcting generating program and the error-correcting program are transferred from the non-volatile memory, and wherein the central processing unit executes the error-correcting information generating program and the error-correcting program transferred to the RAM.

13.   (Original) The data processing system according to claim 12, wherein the central processing unit transfers the error-correcting information generating program and the error-correcting program from the non-volatile memory to the RAM in response to reset instructions.

14.   (Original) The data processing system according to claim 5, further including a RAM accessible by the central processing unit, and wherein the central processing unit successively reads data with error correcting information from the partial storage area of the non-volatile memory in response to reset instructions, effects the error decision and error correction on the read data with error correcting information according to the

execution of the error-correcting program, and initially stores the data subjected to the error decision and correction in the RAM.

15. (Original) The data processing system according to claim 5, wherein the central processing unit has means for holding information indicative of the occurrence of an error uncorrectable in the error determining process under the execution of the error-correcting program, recognizably from the outside.

16. (Currently Amended) A data processing system comprising:

a first storage area which is structured to allow for a relatively low in the number of rewrite assurances; and

a second storage area which is structured to allow for a relatively high in the number of rewrite assurances,

wherein both being provided of said first storage area and second storage area are allocated in an address space of an arithmetic control device,

wherein the first storage area comprises programs which include an ECC code generating program for generating each of ECC codes for data to be written in the second storage area, and an error-correcting program for effecting an error decision and an error correction on data with the ECC codes read from the second storage area,

wherein said second storage area stores data and the ECC code for the data, and

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wherein the arithmetic control device executes the ECC code generating program when data is stored in the second storage area.

17.   (Original) The data processing system according to claim 16, wherein the arithmetic control device executes the error-correcting program when ~~the~~ corresponding data is read from the second storage area.

18.   (Currently Amended) The data processing system according to claim 16, wherein the arithmetic control device ~~is capable of executing~~ executes the error-correcting program in response to a predetermined operation mode and sequentially ~~transferring~~ transfers the data of the second storage area to [[the]] RAM ~~in advance~~.

19.   (Currently Amended) The data processing system according to claim 16, wherein the first storage area is ~~a mask ROM, and~~ arranged in a memory array that is different from the second storage area ~~is an electrically erasable and programmable flash memory~~.

20.   (Original) The data processing system according to claim 16, wherein each of the first storage area and the second storage area is an electrically erasable and programmable flash memory, the flash memory has a write/erase program for the flash memory, and further including a RAM to which the write/erase program is

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transferred from the flash memory, and wherein the
arithmetic control device is capable of executing the
write/erase program placed on the RAM in response to a
specific operation mode.

21.   (Currently Amended) [[A]]The data processing
method using system according to claim 16,

        wherein the ECC code generating program uses a matrix
table wherein when ECC codes are defined as m bits with
respect to data of n bits, mutually-different binary
numbers of m bits are arranged in an m+n array, comprising:
and

        wherein the ECC code generating program performs the
following operations:

        exclusive-ORing values in columns of the matrix table,
corresponding to bit positions of logical values "1" of
data every bits as viewed in a row direction upon
generating the ECC codes;

        setting the values of m bits obtained from the
exclusive-ORing as the ECC codes; and

        adding the ECC codes to data respectively to thereby
generate code words of m+n bits.

22.   (Currently Amended) The data processing method
system according to claim 21, further comprising having the
following operations:

        exclusive-ORing values in columns of the matrix table,
corresponding to bit positions of logical values "1" of the

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code words ~~every bits~~ as viewed in the row direction,
making an error-free decision when the values of m bits
obtained by the exclusive-ORing are of a logical value "0"
in all bits to thereby set the n-bit data of the ~~cord~~ _code_
words as normal data, determining that an error exists when
the values of m bits obtained by the exclusive-ORing are of
a logical value "1" ~~even~~ _for at least_ one bit, retrieving a
column coincident with a binary number of m bits obtained
by the exclusive-ORing from the columns of the matrix
table, inverting bits of code words at positions associated
with the retrieved column in logical value and correcting
the same, and defining the n-bit data of the corrected code
words as normal data.

23. (Original) The data processing system according
to claim 7, wherein the central processing unit has a
storage circuit for holding, when error-correctable data is
detected during the execution of the error-correcting
program, information corresponding to the result of
detection.

24. (Original) The data processing system according
to claim 23, wherein the information corresponding to the
result of detection is used as warning information.

25. (Currently Amended) A semiconductor integrated
circuit comprising:
    a CPU; and

an erasable and programmable non-volatile memory[[;]]~

wherein said memory comprises a plurality of memory areas each of which has a plurality of memory cells,

wherein the CPU ~~is capable of storing one~~ stores data in memory cells at different addresses in a first memory area when information is written in ~~a specific block corresponding to part of storage area in~~ said first memory area of the non-volatile memory,

wherein the CPU stores second data to memory cells at different addresses in a second memory area of the non-volatile memory when information is written in said second memory area of the non-volatile memory, and

~~reading~~ wherein for the first memory area, but not the second memory area, the CPU reads data from the memory cells at the different addresses ~~when data is read from the specific block~~, and ~~performing~~ performs a logical operation on the read plural data to thereby effect a necessary error correction to the data.

26.   (Original) The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is two or more, and the logical operation is a logical OR operation based on the execution of an instruction included in an instruction set of the CPU.

27.   (Original) The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is two or more, and the logical operation is a

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logical AND operation based on the execution of an instruction included in an instruction set of the CPU.

28. (Original) The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is three or more, and the logical operation is an operation for effecting majority decision on the plural data read from the memory cells at the different addresses.

29. (Currently Amended) The semiconductor integrated circuit according to claim 25, wherein the non-volatile memory has a program area for storing a program executed by the CPU, as an area different from the ~~specific block~~ first memory area.

30. (Original) The semiconductor integrated circuit according to claim 29, wherein the program area includes a program for storing the one data in the memory cells at the different addresses, a program for performing the error correction, and other programs.

31. (Currently Amended) The semiconductor integrated circuit according to claim 25, wherein the ~~specific block~~ first memory area has a product ~~spec~~ specification for assuring the number of rewritings greater than other blocks.

32. (Currently Amended) The semiconductor integrated circuit according to claim 25, wherein the non-volatile memory is a flash memory ~~capable of storing~~ that stores information therein according to high and low levels of a threshold voltage of each memory cell.

33. (Original) The semiconductor integrated circuit according to claim 25, wherein the CPU and the non-volatile memory are formed on a single semiconductor chip which constitutes a microcomputer.

34. (Original) The semiconductor integrated circuit according to claim 25, wherein the CPU and the non-volatile memory are respectively formed on separate semiconductor chips.

35. (New) The data processing system according to claim 1, which is a single chip type microcomputer wherein said memory and the central processing unit are formed on a single semiconductor chip.

36. (New) The data processing system according to claim 1, which is configured in a multi-chip form wherein said memory and the central processing unit are respectively formed on discrete semiconductor chips.

37. (New) The data processing system according to claim 1, wherein the first write operation comprises an

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error-correcting information generating operation for generating error correcting information for the data written into the first area of the non-volatile memory, and

wherein a read operation includes an error-correcting operation for effecting an error decision and an error correction on data with error correcting information read from the first area.

38.   (New) The data processing system according to claim 37, which has a storage area for a matrix table wherein when the data is configured as n bits and error correcting information for the n-bit data is defined as m bits, mutually-different binary numbers of m bits are arranged in an m+n array, and wherein the matrix table is referred to the error-correcting information generating operation and the error-correcting operation.

39.   (New) The data processing system according to claim 37, further including a mask ROM accessible by the central processing unit, and wherein the mask ROM has the error-correcting information generating operation and the error-correcting operation.

40.   (New) The data processing system according to claim 37, wherein the other storage areas of the non-volatile memory have areas for storing the error-correcting information generating operation and the error-correcting operation.

41. (New) The data processing system according to claim 40, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed, and the areas for storing the error-correcting information generating operation and the error-correcting operation are assigned to the erase prohibition area.

42. (New) The data processing system according to claim 41, wherein the error-correcting information generating operation serves so as to generate error correcting information and thereafter store the generated error correcting information and data corresponding thereto in the first memory area in accordance with a prescribed format as data with the error correcting information, and the error-correcting operation serves so as to recognize the data with the error correcting information in accordance with the prescribed format.

43. (New) The data processing system according to claim 40, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed, and wherein the areas for storing the error-correcting information

generating operation and the error-correcting operation are assigned to the rewrite allowable area.

44. (New) The data processing system according to claim 37, further including a RAM to which the error-correcting generating operation and the error-correcting operation are transferred from the non-volatile memory, and wherein the central processing unit executes the error-correcting information generating operation and the error-correcting operation transferred to the RAM.

45. (New) The data processing system according to claim 44, wherein the central processing unit transfers the error-correcting information generating operation and the error-correcting operation from the non-volatile memory to the RAM in response to reset instructions.

46. (New) The data processing system according to claim 37, further including a RAM accessible by the central processing unit, and wherein the central processing unit successively reads data with error correcting information from the first memory area of the non-volatile memory in response to reset instructions, effects the error decision and error correction on the read data with error correcting information according to the execution of the error-correcting operation, and initially stores the data subjected to the error decision and correction in the RAM.

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47. (New) The data processing system according to claim 35, wherein the central processing unit has means for holding information indicative of the occurrence of an error uncorrectable in the error determining process under the execution of the error-correcting program, recognizably from the outside.